

DDR3 Registered DIMM

DDR3 Registered DIMM is high-speed, low power memory module that use DDR3 SDRAM in FBGA package, 1 pcs register in TFBGA package and a 2048 bits serial EEPROM on a 240-pin printed circuit board. DDR3 Registered DIMM is a Dual In-Line Memory Module and is intended for mounting into 240-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operation frequencies, programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.



Features

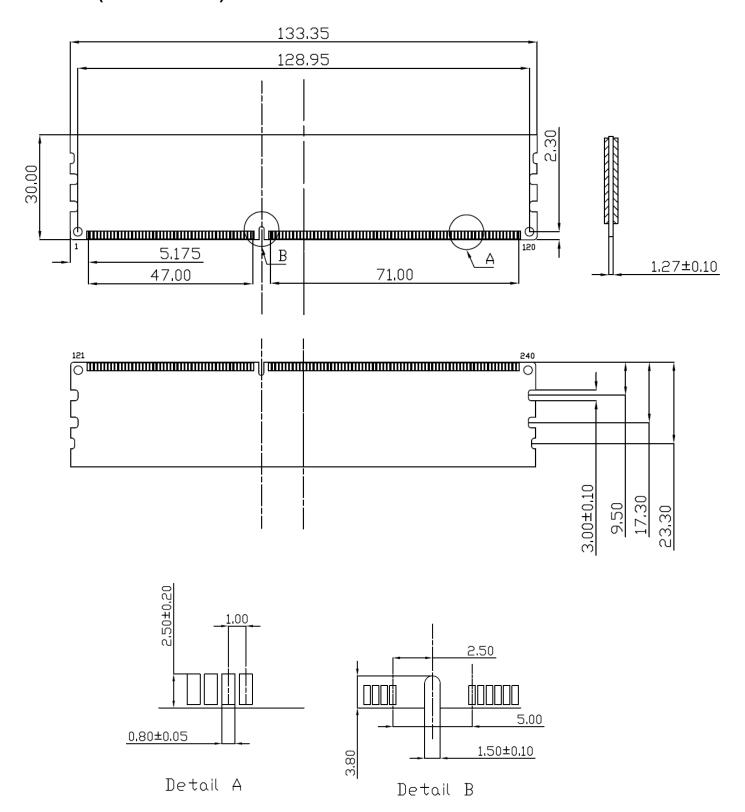
- RoHS compliant products.
- JEDEC standard 1.5V ± 0.075V Power supply
- VDDQ=1.5V ± 0.075V
- Clock Freq: 533MHZ for 1066Mb/s/Pin 667MHZ for 1333Mb/s/Pin. 800MHZ for 1600Mb/s/Pin.
- Programmable CAS Latency: 6, 7, 8, 9, 10, 11
- Programmable Additive Latency (Posted /CAS):
 0,CL-2 or CL-1 clock
- Programmable /CAS Write Latency (CWL)
 = 6 (DDR3-1066), 7 (DDR3-1333), 8 (DDR3-1600)
- 8 bit pre-fetch
- Burst Length: 4, 8
- Bi-directional Differential Data-Strobe
- On DIMM thermal Sensor
- Internal calibration through ZQ pin
- On Die Termination with ODT pin
- Serial presence detect with EEPROM
- Asynchronous reset

Pin Identification

Symbol	Function				
A0~A15, BA0~BA2	Address/Bank input				
DQ0~DQ63	Bi-direction data bus.				
DQS0~DQS8, /DQS0~/DQS8	Data strobes				
CB0~CB7	Data Check Bits				
Par-In	Parity bit for address and Control bus				
CK0, /CK0	Clock Input. (Differential pair)				
CKE0, CKE1	Clock Enable Input.				
ODT0, ODT1	On-die termination control line				
/S0, /S1, /S2, /S3	DIMM rank select lines.				
/RAS	Row address strobe				
/CAS	Column address strobe				
WE	Write Enable				
DM0~DM8	Data masks/high data strobes				
VDD	Core power supply				
VSS	Ground				
$V_{REF}DQ$, $V_{REF}CA$	I/O reference supply				
/ERROUT	Parity error found on address and control bus				
$V_{DD}SPD$	SPD EEPROM power supply				
SA0~SA2	Address select for EEPROM				
SCL	Clock for EEPROM				
SDA	Data for EEPROM				
/EVENT	Temperature Event Pin				
/RESET	Set DRAMs Known State				
VTT	SDRAM I/O termination supply				
NC	No Connection				



Dimensions (Unit: millimeter)



Note:

1. Tolerances on all dimensions +/-0.15mm unless otherwise specified.



Pin Assignments

Pin	Pin	Pin	Pin	Pin	Pin	Pin	Pin	Pin	Pin	Pin	Pin
No	Name	No	Name	No	Name	No	Name	No	Name	No	Name
01	VREFDQ	41	VSS	81	DQ32	121	VSS	161	TDQS17	201	DQ37
02	VSS	42	/DQS8	82	DQ33	122	DQ4	162	/TDQS17	202	VSS
03	DQO	43	DQS8	83	VSS	123	DQ5	163	VSS	203	TDQS13
04	DQ1	44	VSS	84	/DQS4	124	VSS	164	CB6	204	/TDQS13
05	VSS	45	CB2	85	DQS4	125	TDQS9	165	CB7	205	VSS
06	/DQS0	46	CB3	86	VSS	126	/TDQS9	166	VSS	206	DQ38
07	DQSO	47	VSS	87	DQ34	127	VSS	167	NC	207	DQ39
08	VSS	48	VTT	88	DQ35	128	DQ6	168	/RESET	208	VSS
09	DQ2	49	VTT	89	VSS	129	DQ7	169	CKE1,NC	209	DQ44
10	DQ3	50	CKE0	90	DQ40	130	VSS	170	VDD	210	DQ45
11	VSS	51	VDD	91	DQ41	131	DQ12	171	A15	211	VSS
12	DQ8	52	BA2	92	VSS	132	DQ13	172	A14	212	TDQS14
13	DQ9	53	/Err_ Out	93	/DQS5	133	VSS	173	VDD	213	/TQS14
14	VSS	54	VDD	94	DQS5	134	TDQS10	174	A12	214	VSS
15	/DQS1	55	A11	95	VSS	135	/TDQS10	175	A9	215	DQ46
16	DQS1	56	A7	96	DQ42	136	VSS	176	VDD	216	DQ47
17	VSS	57	VDD	97	DQ43	137	DQ14	177	A8	217	VSS
18	DQ10	58	A5	98	VSS	138	DQ15	178	A6	218	DQ52
19	DQ11	59	A4	99	DQ48	139	VSS	179	VDD	219	DQ53
20	VSS	60	VDD	100	DQ49	140	DQ20	180	A3	220	VSS
21	DQ16	61	A2	101	VSS	141	DQ21	181	A1	221	TDQS15
22	DQ17	62	VDD	102	/DQS6	142	VSS	182	VDD	222	/TDQS15
23	VSS	63	NC	103	DQS6	143	TDQS11	183	VDD	223	VSS
24	/DQS2	64	NC	104	VSS	144	/TDQS11	184	CKO	224	DQ54
25	DQS2	65	VDD	105	DQ50	145	VSS	185	/CKO	225	DQ55
26	VSS	66	VDD	106	DQ51	146	DQ22	186	VDD	226	VSS
27	DQ18	67	VREFCA	107	VSS	147	DQ23	187	/EVENT	227	DQ60
28	DQ19	68	Par-In	108	DQ56	148	VSS	188	A0	228	DQ61
29	VSS	69	VDD	109	DQ57	149	DQ28	189	VDD	229	VSS
30	DQ24	70	A10/AP	110	VSS	150	DQ29	190	BA1	230	TDQS16
31	DQ25	71	BA0	111	/DQS7	151	VSS	191	VDD	231	/TDQS16
32	VSS	72	VDD	112	DQS7	152	TDQS12	192	/RAS	232	VSS
33	/DQS3	73	WE	113	VSS	153	/TDQS12	193	/S0	233	DQ62
34	DQS3	74	/CAS	114	DQ58	154	VSS	194	VDD	234	DQ63
35	VSS	75	VDD	115	DQ59	155	DQ30	195	ODTO	235	VSS
36	DQ26	76	/S1	116	VSS	156	DQ31	196	A13	236	VDDSPD
37	DQ27	77	ODT1,NC	117	SA0	157	VSS	197	VDD	237	SA1
38	VSS	78	VDĎ	118	SCL	158	CB4	198	/S3,NC	238	SDA
39	CB0	79	/S2,NC	119	SA2	159	CB5	199	VSS	239	VSS
40	CB1	80	VSS	120	VTT	160	VSS	200	DQ36	240	VTT